NEIFELD IP LAW, P.C.
2001 Jefferson Davis Highway
Suite 1001, Crystal Plaza 1
Arlington, VA 22202

Tel: 703-415-0012
Fax: 703-415-0013
Email: rneifeld@Neifeld.com
Web: www.Neifeld.com

TRANSMITTAL LETTER

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

Neifeld Ref.: OSEM0001
In Re Application of: PASSLACK
USPTO Confirmation Code:
Serial No: 09/022,593
Filed: February 12, 1998
Now USP: 5,945,718 Issued August 31, 1999
Examiner: Hardy; David B.
For: Self-aligned metal-oxide-compound semiconductor device and method of fabrication

SIR:

Attached hereto for filing are the following papers:

37 CFR 1.501 SUBMISSION OF A REFERENCE INTO THE FILE OF AN ISSUED PATENT. (4 PAGES)
CERTIFICATE OF SERVICE (1 PAGE)
ATTACHMENT 1

Our check in the amount of $0.00 is attached covering the required fees.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-2106.

31518
31518
PATENT TRADEMARK OFFICE

10/19/04
Date

Richard A. Neifeld, Ph.D.
Registration No. 35,299
Attorney of Record

Y:\Clients\Osemi\OSEM0001\Documents\TransLtr_041014.wpd

NEIFELD REF.: OSEM0001

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: PASSLACK

USPTO CONFIRMATION CODE:

SERIAL NO: 09/022,593

FILED: FEBRUARY 12, 1998

NOW USP: 5,945,718 ISSUED AUGUST 31, 1999

EXAMINER: Hardy; David B.

FOR: Self-aligned metal-oxide-compound semiconductor device and method of fabrication

37 CFR 1.501 SUBMISSION

OF A REFERENCE INTO THE FILE OF AN ISSUED PATENT

ASSISTANT COMMISSIONER FOR PATENTS

ALEXANDRIA, VA 22313

Sir: Please enter this paper and the attached prior art reference into the file for USP 5,945,718. The following pages show compliance with 37 CFR 1.501, including certification of service.

COMPLIANCE WITH 37 CFR 1.501

I. **37 CFR1.501(a)**

37 CFR 1.501 is entitled "§ 1.501 Citation of prior art in patent files."

37 CFR 1.501(a) states that:

> (a) At any time during the period of enforceability of a patent, any person may cite, to the Office in writing, prior art consisting of patents or printed publications which that person states to be pertinent and applicable to the patent and believes to have a bearing on the patentability of any claim of the patent. If the citation is made by the patent owner, the explanation of pertinency and applicability may include an explanation of how the claims differ from the prior art. Such citations shall be entered in the patent file except as set forth in §§ 1.502 and 1.902. [46 FR 29185, May 29, 1981, effective July 1, 1981; para. (a) revised, 65 FR 76756, Dec. 7, 2000, effective Feb. 5, 2001.]

I believe that the reference Passlack, et al, "Low Dit, Thermondynamically Stable Ga2O3-GaAs Interfaces: Fabrication, Characterization, and Modeling", IEEE Transactions on Electron Devices, Vol. 44, No. 2 February 1997 to "be pertinent and applicable to the patent and ... to have a bearing on the patentability of any claim of the patent."[1]

I do not represent the patent owner.

II. **37 CFR 1.501(b)**

37 CFR 1.501(b) states that:

> (b) If the person making the citation wishes his or her identity to be excluded from the patent file and kept confidential, the citation papers must be submitted

---

[1]Attachment 1 is a copy of Passlack, et al, "Low Dit, Thermondynamically Stable Ga2O3-GaAs Interfaces: Fabrication, Characterization, and Modeling", IEEE Transactions on Electron Devices, Vol. 44, No. 2 February 1997.

without any identification of the person making the submission. [46 FR 29185, May 29, 1981, effective July 1, 1981; para. (a) revised, 65 FR 76756, Dec. 7, 2000, effective Feb. 5, 2001.]

Section 37 CFR 1.501(b) is not relevant.

III. **37 CFR 1.501(c)**

37 CFR 1.501(c) states that:

(c) Citation of patents or printed publications by the public in patent files should either: (1) Reflect that a copy of the same has been mailed to the patent owner at the address as provided for in § 1.33(c); or in the event service is not possible (2) Be filed with the Office in duplicate. [46 FR 29185, May 29, 1981, effective July 1, 1981; para. (a) revised, 65 FR 76756, Dec. 7, 2000, effective Feb. 5, 2001.]

I am serving a copy of this paper and the listed attachment on the address of record for USP 5,945,718. The USPTO's assignment records database indicates that the address as provided for in § 1.33(c) is:

MOTOROLA, INC.
GREGORY J. GORRIE
INTELLECTUAL PROPERTY DEPT., SUITE R3108
P.O. BOX 10219
SCOTTSDALE, ARIZONA 85271-0219

The citations to 37 CFR 1.501 are based upon the version identified by:

Respectfully Submitted, 10/19/04

DATE

Richard A. Neifeld, Ph.D.

Registration No. 35,299

Printed: October 19, 2004 (9:57am)

Y:\Clients\Osemi\OSEM0001\OSEM0001_Motorola_Passlack\37_CFR1_501_USP5945718_PASSLACK_041014.wpd

CERTIFICATE OF SERVICE:

A copy of this document and the noted attachments are being mailed by first class mail to:

MOTOROLA, INC.
GREGORY J. GORRIE
INTELLECTUAL PROPERTY DEPT., SUITE R3108
P.O. BOX 10219
SCOTTSDALE, ARIZONA 85271-0219

Printed: October 19, 2004 (9:57am)
Y:\Clients\Osemi\OSEM0001\OSEM0001_Motorola_Passlack\37_CFR1_501_USP5945718_PASSLACK_041014.wpd

Attachment 1

Low D_{it}, Thermodynamically Stable Ga_2O_3–GaAs Interfaces: Fabrication, Characterization, and Modeling

M. Passlack, *Member, IEEE*, M. Hong, *Member, IEEE*, J. P. Mannaerts, R. L. Opila, *Member, IEEE*, S. N. G. Chu, N. Moriya, F. Ren, *Senior Member, IEEE*, and J. R. Kwo

Abstract— **Thermodynamically stable, low D_{it} amorphous Ga_2O_3-(100) GaAs interfaces have been fabricated by extending molecular beam epitaxy (MBE) related techniques. We have investigated both *in situ* and *ex situ* Ga_2O_3 deposition schemes utilizing molecular beams of gallium oxide. The *in situ* technique employs Ga_2O_3 deposition on freshly grown, atomically ordered (100) GaAs epitaxial films in ultrahigh vacuum (UHV); the *ex situ* approach is based on thermal desorption of native GaAs oxides in UHV prior to Ga_2O_3 deposition. Unique electronic interface properties have been demonstrated for *in situ* fabricated Ga_2O_3–GaAs interfaces including a midgap interface state density D_{it} in the low 10^{10} cm^{-2} eV^{-1} range and an interface recombination velocity S of 4000 cm/s. The existence of strong inversion in both n- and p-type GaAs has been clearly established. We will also discuss the excellent thermodynamic and photochemical interface stability. *Ex situ* fabricated Ga_2O_3–GaAs interfaces are inferior but still of a high quality with S = 9000 cm/s and a corresponding D_{it} in the upper 10^{10} $cm^{-2}eV^{-1}$ range.**

We also developed a new numerical heterostructure model for the evaluation of capacitance–voltage (C–V), conductance–voltage (G–V), and photoluminescence (PL) data. The model involves selfconsistent interface analysis of electrical and optoelectronic measurement data and is tailored to the specifics of GaAs such as band-to-band luminescence and long minority carrier response time τ_R. We will further discuss equivalent circuits in strong inversion considering minority carrier generation using low-intensity light illumination.

I. Introduction

LOW-POWER technologies are key to the widespread use of high-performance portable systems such as portable computers, cellular telephones, personal communicators, PDA's, medical devices, etc. At the present time, bulk Si CMOS offers significant advantages in terms of integration level and cost; however, reductions in circuit speed of bulk Si CMOS are anticipated as the power supply is scaled to 1 V or below [1], [2]. The decrease in circuit speed can be compensated only to a certain extent by innovative technologies (e.g., silicon on insulator [3]) and parallel architectures or pipelining (e.g., [4]). Consequently, the natural choice for low-power, high-speed/frequency devices remain technologies using high-mobility materials such as GaAs and related compounds (e.g., [5], [6]). Complementary GaAs technologies exhibit advantages over bulk Si such as low parasitic capacitance and process simplicity similar to SOI. Beyond the improvements provided by SOI, high-mobility technologies also offer very low "on" voltage and high transconductance at low voltage resulting in optimum speed/power performance at supply voltages of 1 V and below. At low supply voltages, complementary GaAs technologies have demonstrated a 4–9 times lower power consumption with the same gate delay when compared to SOI [5]. Further, high transconductance is essential for minimizing interconnect delay [7]. One of the key remaining issues for GaAs, however, is the lack of insulating layers providing low D_{it} and stable device operation. The use of MODFET's in present complementary GaAs technologies causes excessive gate leakage currents and results in unacceptable high stand-by power for portable systems. Gate leakage also affects the gain and limits the maximum output power in power amplifiers using a single power supply.

This paper presents an approach to overcome the above described bottleneck of insulating layers on GaAs providing low D_{it} and stable device operation. We will illustrate how the extension of MBE toward deposition of gallium oxide molecules has provided the required ingredients for the implementation of thermodynamically stable, low D_{it} oxide-GaAs interfaces. Pivotal aspects include an extremely low GaAs surface exposure to impurities (<10–100 Langmuirs, $1L = 10^{-6}$ torr s) and the preservation of GaAs bulk and surface stoichiometry [8], the complete exclusion of GaAs surface oxidation [9]–[11], and the requirement of a specific atomic structure associated with the interfacial atoms of GaAs and the deposited molecules [12]. We will emphasize that these requirements are met when specific molecules are deposited *in situ* under ultrahigh vacuum conditions. Further, we will discuss first results obtained using an *ex situ* deposition scheme which is applicable to GaAs surfaces exposed to room air and/or processing environments during fabrication of devices.

Manuscript received July 2, 1996; revised September 17, 1996. The review of this paper was arranged by Editor J. Xu. M. Passlack's work was supported in part by the Deutsche Forschungsgemeinschaft.

M. Passlack was with AT&T Bell Laboratories, Murray Hill, NJ 07974 USA. He is now with Motorola Inc., Phoenix Corporate Research Laboratories, Tempe, AZ 85284 USA.

M. Hong, J. P. Mannaerts, R. L. Opila, S. N. G. Chu, F. Ren, and J. R. Kwo are with Bell Laboratories, Lucent Technologies, Murray Hill, NJ 07974 USA.

N. Moriya was with AT&T Bell Laboratories, Murray Hill, NJ 07974 USA. He is now with Netmor Ltd.—Applied Modeling Research, Tel Aviv 61390, Israel.

Publisher Item Identifier S 0018-9383(97)00894-0.

The following sections will cover *in situ* and *ex situ* wafer fabrication, interface characterization, and modeling.

II. Wafer Fabrication

The 2–in wafers were fabricated using a multiple-chamber UHV system [13]. The wafer fabrication was comprised of 1.5-μm thick n-type (1.6×10^{16} cm^{-3}) or p-type (4.4×10^{16} cm^{-3}) GaAs epilayers grown by solid source MBE on heavily Si or Zn-doped (100) GaAs substrates, respectively. After completion of GaAs growth, *in situ* and *ex situ* schemes were investigated as described in the following paragraphs.

A. In Situ Deposition

After completion of GaAs growth, the freshly grown film with an As-stabilized (2×4) surface was transferred under a vacuum of 6×10^{-11} torr to another chamber (background pressure = 10^{-10} torr) for oxide deposition. Fig. 1 shows the pressure (solid line) and the corresponding GaAs surface exposure (dashed line) which is typically observed prior to opening the shutter for oxide deposition. The time t_c and t_s is the time of completion of GaAs growth and the time at which the shutter was opened for oxide deposition, respectively. The GaAs surface was exposed to a pressure not higher than 10^{-10} torr during the transfer and heating of the substrate to the deposition temperature T_s. For the last 2 min, the e-beam was turned on to heat up the oxide target. Only then did the GaAs surface begin to experience the pressure from 10^{-10} to 10^{-7} torr. The pressure rise (predominantly oxygen) was caused by vaporization and thermal dissociation of the oxide targets during e-beam heating. Note that the typical GaAs surface exposure prior to opening the shutter for oxide deposition ($t_c < t < t_s$) was $\leq$10 Langmuirs. Based on typical initial sticking coefficients for oxygen (e.g., [14]), the GaAs surface impurity coverage is estimated at 10^{-5}–10^{-3}% of a mono-layer or 10^8–10^{10} surface impurities/cm^2 prior to deposition.

The preservation of surface periodicity and atomic order was investigated by *in situ* reflection high-energy electron diffraction (RHEED) in the time interval $t_c < t < t_s$. RHEED pictures acquired from a (100) GaAs surface at the time t_c and t_s(T_s = 360 °C) are identical, showing a (2×4) reconstructed, As-stabilized surface (Fig. 2). The surface reconstruction (2×4) and long streaky RHEED patterns indicate an atomically ordered and contamination free surface. Consequently, the surface atomic order and periodicity is not affected by exposure to impurity gases of less than 10 Langmuirs in our experiments and the surface stoichiometry is completely preserved prior to opening the shutter for oxide deposition at time t_s.

B. Ex Situ Deposition

Here, the wafers were removed from the MBE chamber after completion of GaAs growth, exposed to room air for at least three days, and then loaded into the oxide deposition chamber (background pressure = 10^{-10} torr). The native

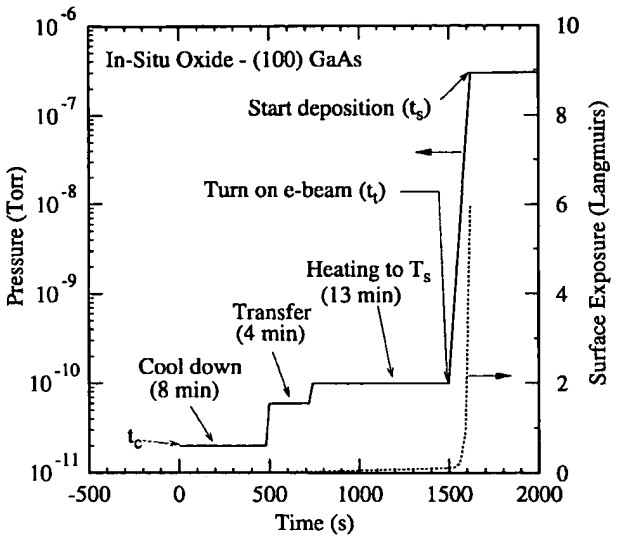


Fig. 1. Pressure (solid line) and surface exposure (dashed line) measured between completion of GaAs epitaxial growth (t_c) and start of oxide deposition (t_s).

oxides which built up on the GaAs surface during air exposure were thermally desorbed without As overpressure at a substrate temperature T_s of 580–600 °C. RHEED was used to monitor the process of native oxide desorption. No surface reconstruction was observed and the RHEED streaks were not continuous [15]. The latter is indicative of surface roughness and residual contamination.

Finally, oxide films were deposited at substrate temperatures T_s ranging from room temperature to $\cong$ 600 °C using molecular beams of gallium oxide. Single crystal $Gd_3Ga_5O_{12}$ [16] was used as a source material and evaporated by an e-beam technique. The use of $Gd_3Ga_5O_{12}$ was motivated by the unavailability of single crystal Ga_2O_3 and had led to the first successful deposition of gallium oxide molecules forming very uniform Ga_2O_3 films on GaAs [17]. Note that Ga_2O_3 exhibits a high sublimation temperature of 1725 °C [18]. The fabrication of MOS capacitors was completed by deposition of Ti/Au metal dots using a standard shadow mask process.

Reference wafers with identical GaAs epitaxial structure and substrate were also fabricated in the same solid-source III–V chamber using 1) no oxide deposition (bare samples), and 2) $Al_{0.45}Ga_{0.55}As$ interfaces.

III. Structural Properties

The chemical composition of Ga_2O_3–GaAs interfaces has been investigated by X-ray photoelectron spectroscopy (XPS). Compositional profiles and the crystallographic structure of the deposited oxide films have been studied by Rutherford backscattering spectrometry (RBS), secondary ion mass spectroscopy (SIMS), transmission electron microscopy (TEM), and RHEED, respectively.

Fig. 3 shows measured (solid line) and simulated (dashed line) RBS spectra of a gallium oxide film deposited *in situ* on GaAs at T_s = 360 °C. The ratio of Ga with oxygen was determined to 43:55.5. Previously published results indicated

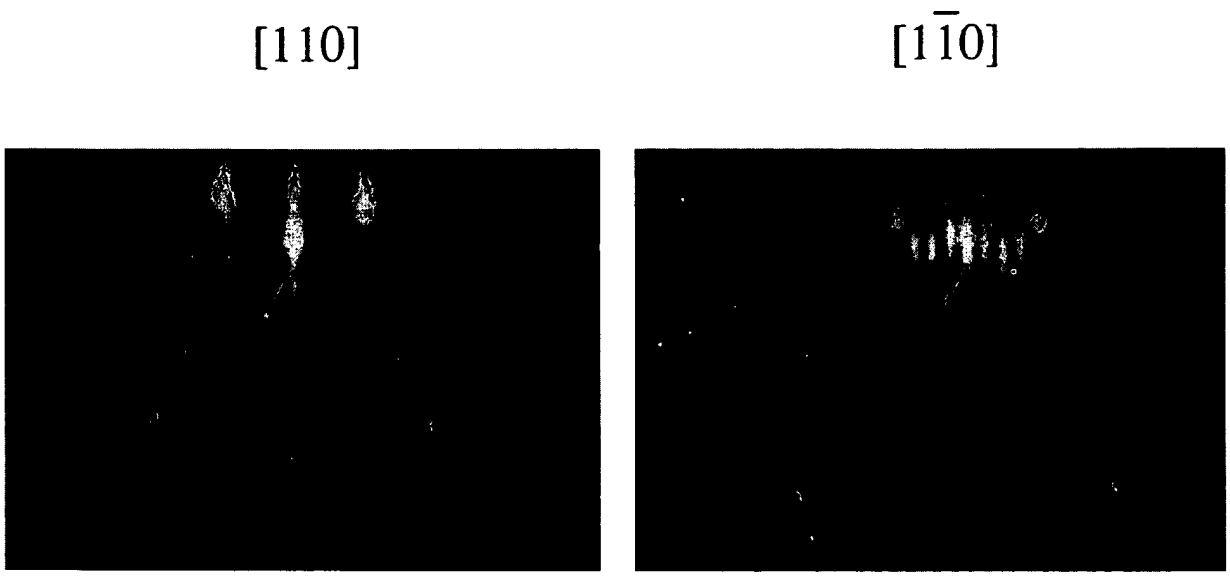


Fig. 2. Identical RHEED picture taken at time t_c and t_s. The RHEED picture shows a (2 × 4) reconstructed surface indicating preservation of surface atomic order and stoichiometry.

that the nonstoichiometry of the Ga_2O_3 film is due to incorporation of excess elemental Ga [17]. Further, Ga_2O_3 films using e-beam evaporation of $Gd_3Ga_5O_{12}$ typically exhibit a nonuniform Gd distribution characterized by a virtually Gd free interfacial region and a peak in Gd concentration at the film surface (see Fig. 3). Our characterization methods (including XPS and SIMS) can not completely exclude the presence of Gd at the interface and possible effects of Gd on electronic interface properties are not known at this time. The presence of Gd in the bulk oxide film may affect electrical measurements conducted on MOS structures to be discussed later. In the following, we will refer to the oxide films as Ga_2O_3 films. Fig. 4 shows the plan view TEM micrograph and the corresponding electron diffraction pattern of a Ga_2O_3 film deposited *in situ* on GaAs at $T_s = 360$ °C. As observed from TEM (and RHEED) studies, Ga_2O_3 films are amorphous with partial ordering in a completely disordered state for increased deposition temperature [17], [19]. The amorphous phase of Ga_2O_3 films eludes problems arising from lattice-mismatched interfaces.

Interfacial As 3d core level spectra were acquired using a Perkin Elmer 5600 series XPS spectrometer equipped with a monochromatic Al Kα X-ray source. The photon energy was 1486.6 eV. Depth profiling was done *in situ* in a UHV chamber (background pressure = 5×10^{-10} torr) by Ar sputtering using an ion gun at 4 keV. The sputtering rate of $\cong$ 0.3 nm/cycle has been significantly smaller than the effective photoelectron escape depth of $\cong$ 2 nm [20]. Fig. 5 shows typical interfacial depth profiles of Ga and As 3d core levels of a) *in situ* and b) *ex situ* fabricated Ga_2O_3–GaAs structures. The 3d binding energies of Ga_{GaAs} and As_{GaAs} are identical to standard XPS lines reported earlier (19.2 and 41.2 eV, respectively) [21]. The binding energy of $Ga_{Ga_2O_3}$ is 21.2 and 20.8 eV for *in situ* and *ex situ* fabricated interfaces, respectively. The Ga 3d peak gradually shifts from the bulk

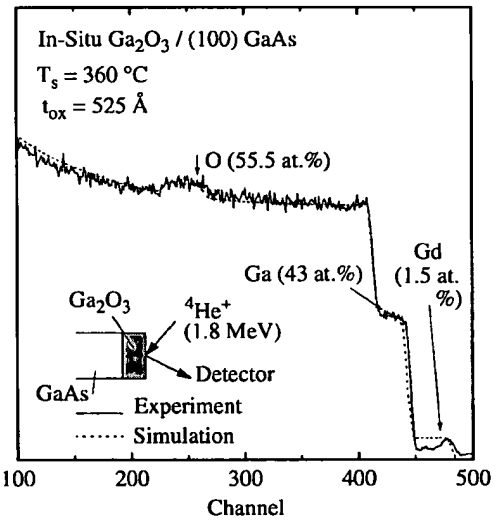


Fig. 3. Measured (solid line) RBS spectrum of 52.5-nm thick Ga_2O_3 film *in situ* deposited on GaAs substrate. The simulation (dashed line) assumes constant Gd concentration throughout the film.

Ga_2O_3 to the bulk GaAs on a length scale consistent with the electron escape depth. The intermediate peak can easily be fitted as a sum of two components. Chemical reaction products, in particular As_2O_3 (44.6 eV) and As_2O_5 (45.7 eV) are not detectable at both *in situ* and *ex situ* fabricated Ga_2O_3–GaAs interfaces. Consequently, the chemical reaction $As_2O_3 + 2$ GaAs $\rightarrow$ $Ga_2O_3 + 4$As ($\Delta G = -62$ kcal/mol) [10] resulting in formation of metallic As and degradation of electronic interface properties [11] is excluded. A more detailed discussion of XPS spectra acquired from Ga_2O_3-GaAs structures is given in [22].

Note that virtually identical, As_xO_y and metallic As free, interfacial As 3d core level profiles were obtained from *in situ* fabricated amorphous Al_2O_3-(100) GaAs and amorphous

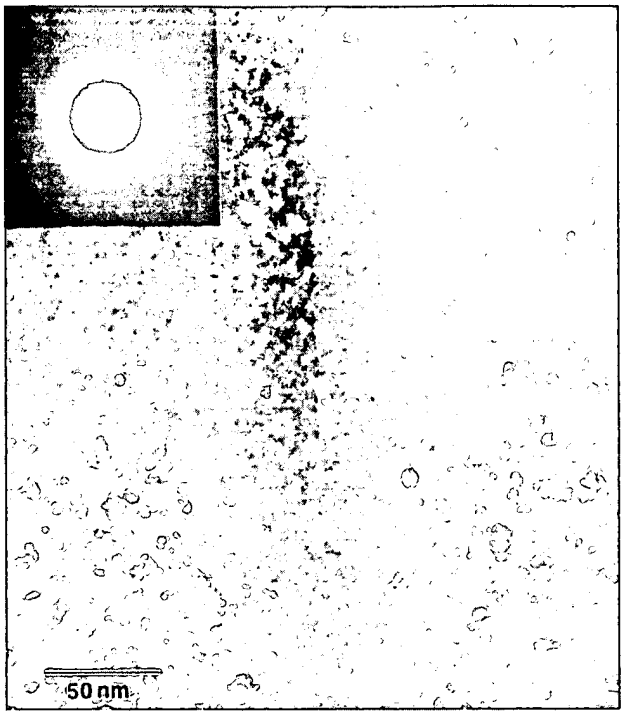


Fig. 4. Plan view TEM and the corresponding electron diffraction pattern of a 26-nm thick Ga_2O_3 film *in situ* deposited on GaAs at 360 °C.

SiO_2-(100) GaAs structures as well. However, in sharp contrast to Ga_2O_3–GaAs interfaces, these interfaces exhibit a surface recombination velocity S comparable to that of a bare surface ($\geq 10^7$cm/s) and a Fermi level pinned at the interface as demonstrated by C–V measurements [12]. Evidently, the absence of As_xO_y and metallic As is a necessary, but not sufficient, requirement for unpinned interfaces on GaAs. We attribute the fundamentally different electronic interface properties observed at various *in situ* fabricated oxide-GaAs interfaces to the specific atomic structure associated with the interfacial atoms of GaAs and the deposited oxide molecules. Therefore, we have chosen the term *intrinsic* pinning for our observation of Fermi level pinning at *in situ* fabricated SiO_2– and Al_2O_3–GaAs interfaces.

IV. Electrical Properties

Electrical properties have been investigated by capacitance–voltage (C–V), conductance–voltage (G–V), and current–voltage (I–V) measurements. Quasi-static and high-frequency (100 kHz, 1 MHz) C–V measurements have been performed on MOS capacitors using a Keithley 590 CV Analyzer, a Keithley 595 Quasi-static CV Meter, and a Keithley 230 Programmable Voltage Source. Further C–V characterizations have been carried out at frequencies of 100 Hz, 1 kHz, and 10 kHz using a Hewlett Packard 4284A Precision LCR Meter. All characterizations were done at room temperature in a shielded probe station. Complementary optoelectronic interface characterizations have been performed using the dependence of the photoluminescence intensity I_{PL} on the incident light power density on the sample surface

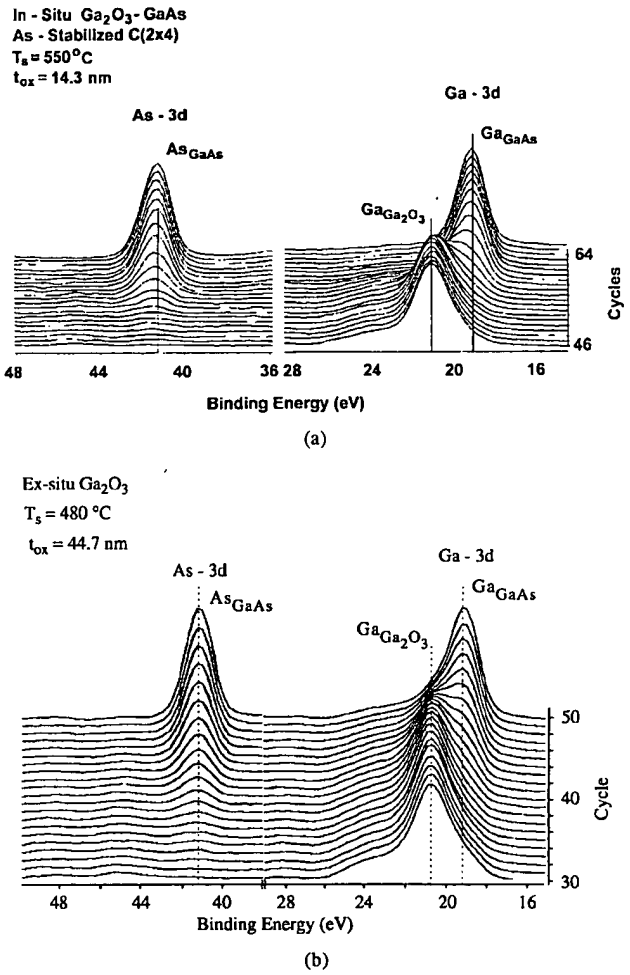


Fig. 5. Interfacial depth profile of Ga and As 3d core levels of as deposited (a) *in situ* and (b) *ex situ* fabricated Ga_2O_3 films. Peak energy positions and full line width at half-maximum (FWHM) are identical to standard values reported earlier [21]. The small structure in the oxide film detectable at $\cong$ 45 eV is associated with the $Gd_{Gd_2O_3}$ 5s line.

P_0. Thorough studies of the internal quantum efficiency η (derived from I_{PL}) over a wide range of P_0 provide the interface recombination velocity S [23]

$$S = \overline{v}_{th}\sigma \int_{E_v}^{E_c} \frac{D_{it}(E)\,dE}{1 + \frac{2n_i}{N}\cosh\frac{E - E_i}{kT}} \tag{1}$$

which is directly related to D_{it} obtained from C–V and G–V measurements. Here, $\overline{v}_{th}$, σ, E_c, E_v, E, n_i, N, E_i, k, and T are the average thermal velocity, the capture cross section of interface states, the conduction and valence band energy, the energy, the intrinsic carrier density, the doping concentration, the intrinsic energy level, the Boltzmann constant, and the temperature in Kelvin, respectively. The advantages of the above outlined η–P_0 technique include the capability to characterize interfaces with extremely thin insulating films, and the exclusion of effects caused by bulk properties of the insulating film. The η–P_0 approach also provides the capture cross section σ independent of G–V characterizations.

Based on conventional numerical models for semiconductor heterostructures (e.g., [24]), we developed a new model which

involves selfconsistent interface analysis of electrical (C–V) and optoelectronic (η–P_0) measurement data and is tailored to the specifics of GaAs such as band-to-band luminescence (photoluminescence) and long minority carrier response time τ_R. The model comprises Poisson's equation and the steady-state continuity equations. Details of the model will be discussed in [25].

Excellent electrical interface properties have been obtained for 350 °C, $\leq T_s \leq$ 600 °C, however, the interface degraded rapidly for $T_s <$ 300 °C. Since the dependence of electrical interface properties on T_s was discussed in [26] for the entire range of deposition temperatures (0–600 °C), we focus on 350 °C $\leq T_s \leq$ 600 °C in the following section.

A. In Situ Deposited Ga_2O_3–GaAs Interfaces

In this section, we discuss measurement results obtained from *in situ* fabricated Ga_2O_3–GaAs structures including C–V, G–V, I–V, and η–P_0 data. D_{it} and S will be derived and we will thoroughly investigate the strong inversion regime which has been observed in GaAs for the first time. Figs. 6 and 7 show typical C–V and G–V characteristics, respectively, of (a) n-type and (b) p-type Ga_2O_3–GaAs MOS structures measured in quasi-static mode and at various frequencies between 100 Hz and 1 MHz. The measured curves have been acquired using low-intensity light illumination ($I_0 = 9.4 \times 10^{14}$ cm^{-2} s^{-1}). Here, I_0 is the incident light intensity on the sample surface. Note that the optical transmissivity T of our metal dots is $\cong 10^{-3}$ resulting in a significantly lower light intensity I_0' entering GaAs. As will be discussed later, low-intensity light illumination is the only viable approach to observe inversion in C–V measurements on epitaxial GaAs due to the small thermal generation/recombination rate of GaAs. We have carefully investigated further effects of low-intensity light illumination, in particular possible implications for the derivation of D_{it}. In Fig. 6, the classical operational modes of ideal MOS structures are clearly revealed and we will discuss the regimes of 1) strong inversion, 2) accumulation, and 3) depletion in the following section. The relative dielectric constant of Ga_2O_3 films obtained by fitting simulation results to the measurement data is 14.2.

1) Strong Inversion: We have investigated different mechanisms of inversion carrier generation/recombination including thermal generation/recombination and low-intensity light generation. Thermal generation/recombination of minority (inversion) carriers is dominated by bulk trap levels E_t near midgap located within the depletion layer where the Fermi level E_F crosses E_t (crossover point [27]). In our structures, the crossover point is located in the lightly doped epitaxial layers which typically exhibit bulk minority carrier lifetimes $\tau_{p,n}$ in excess of 100 ns [23]. The minority carrier response time τ_R for thermal generation/recombination is given by [27]

$$\tau_R = \frac{1}{\sqrt{2}}\left(\frac{N}{n_i}\right)\tau \qquad (2)$$

where $\tau = \sqrt{\tau_n \tau_p}$. With $\tau_p = \tau_n = \tau >$ 100 ns, $n_i = 2.7 \times 10^6$ cm^{-3}, and N in the low 10^{16} cm^{-3} range, (2) gives $\tau_R \geq$ 400 s. Consequently, we did not observe inversion due to thermal generation/recombination in our C–V measurements even at very low sweep rates. Instead, the samples operate in the deep depletion regime with identical high-frequency and quasi-static capacitance [25].

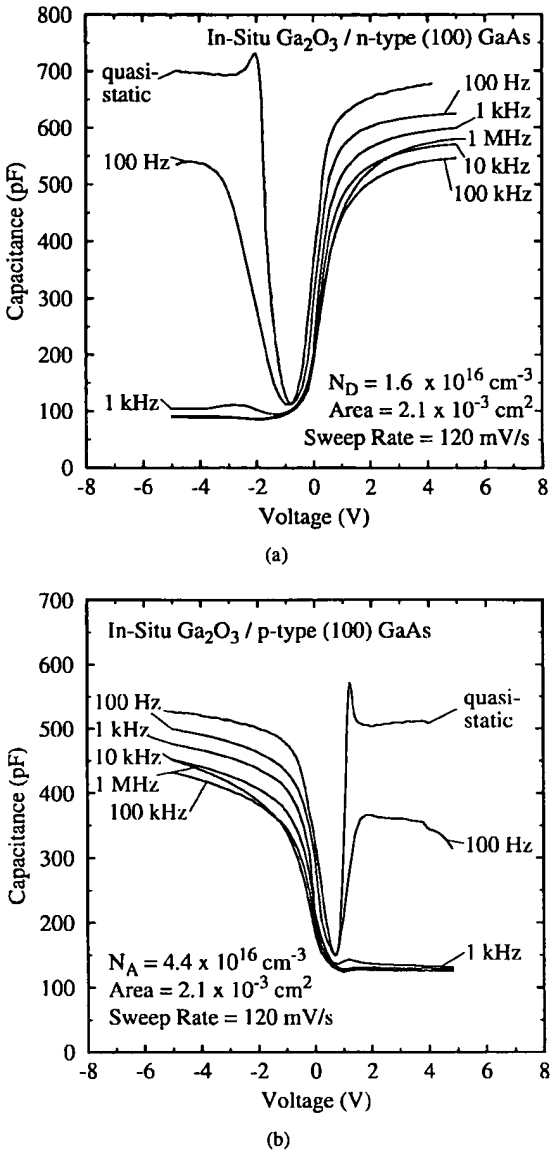


Fig. 6. Typical C–V characteristics of *in situ* fabricated Ga_2O_3–GaAs (a) n-type and (b) p-type samples. Oxide thickness t_{ox} and flatband capacitance C_f are 46.2 nm and 310 pF, and 59.4 nm and 304 pF, respectively. The substrate deposition temperature T_s is $\cong$ 600 °C, the light intensity during the measurement $I_0 = 9.4 \times 10^{14}$ cm^{-2} s^{-1}.

In contrast to thermal generation/recombination, high generation rates can be readily achieved with low-intensity light illumination. Using our standard microscope illumination and objectives with magnification 2, 10, and 20, optical generation rates for electrons and holes $G_n = G_p \equiv I_0(\lambda_0 \leq 870$ nm) ranging from 4.6×10^{13}–2.6×10^{15} cm^{-2} s^{-1} ($12.7 \leq P_0 \leq 715\,\mu$W/cm^2) are obtained. Here, λ_0 is the wavelength of the incident light. Note that a light pulse is also often used for C–V measurements on state-of-the-art SiO_2–Si ($n_i = 1.4 \times 10^{10}$ cm^{-3}) with Si bulk lifetimes of the order of milliseconds in

order to generate minority carriers when the structure is biased in inversion. In our experiments, leakage currents of up to 200 pA [28] corresponding to 6×10^{11} carriers/cm^2 s required steady state low-intensity light illumination to maintain strong inversion.

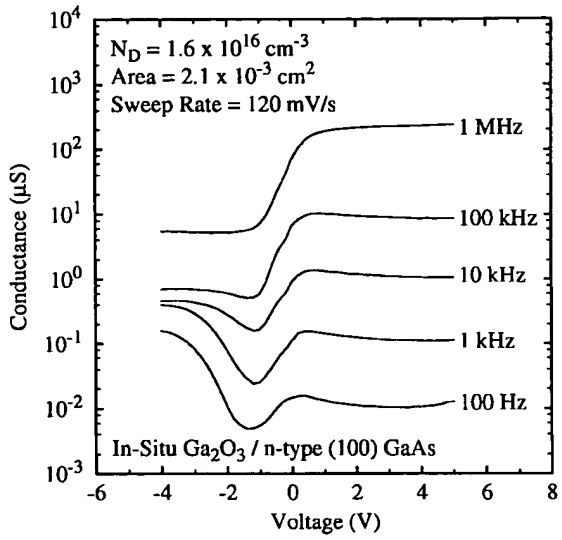
We have further evaluated the measured conductance G in strong inversion (Fig. 7). G is related to the inversion carrier generation/recombination conductance G_{gr} by [27]

$$G = G_{gr} \frac{(\omega C_{ox})^2}{G_{gr}^2 + \omega^2 (C_{ox} + C_D)^2} \tag{3}$$

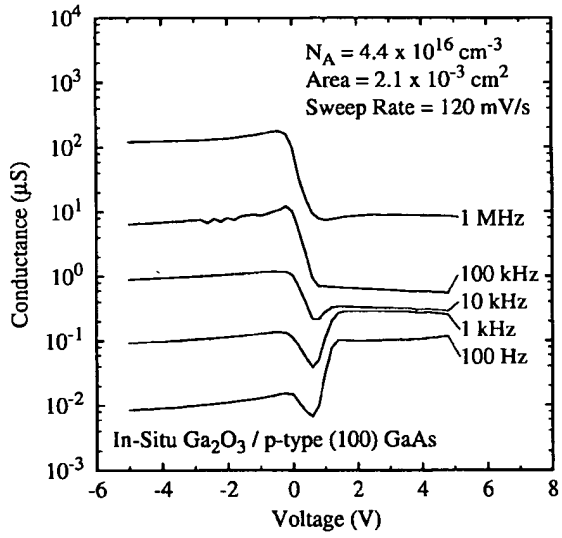
where ω, C_{ox}, and C_D are the angular frequency, the oxide capacitance, and the depletion layer capacitance, respectively. In Fig. 7, G is described by (3) for frequencies $f \leq 10$ kHz. Series resistance loss, which will be discussed later in conjunction with the accumulation regime, significantly increases for $f > 10$ kHz and dominates at high frequencies. G_{gr} is a central component of the MOS equivalent circuit in strong inversion and can be derived from G or from the measured capacitance C in strong inversion [27]. For example, Fig. 8(a) shows the conductance G as a function of frequency with I_0 as a parameter for a Ga_2O_3/p-type GaAs structure in strong inversion. G_{gr} is inferred from the plateaus in the measurement curves using (3) and G_{gr} is plotted as a function of I_0 in Fig. 8(b). Linear G_{gr}–I_0 relations have been obtained with a regression coefficient of 6.7×10^{-16} and 8.3×10^{-16} μS cm^2 s for p- and n-type structures, respectively. Identical values of G_{gr} have been inferred using the frequency ω_m which marks the transition from low-frequency to high-frequency behavior in the measured C–V characteristics [27]. Fig. 8(b) also shows the minority carrier response time $\tau_R = G_{gr}/C_D$. No attempt has been made to theoretically derive an expression for G_{gr} as a function of I_0. Note that G_{gr} does not only depend on the light intensity I_0' entering the semiconductor through the metal dot but is also influenced by minority carriers generated within a diffusion length of the metal dot edge.

The capacitance overshoot at the onset of inversion (Fig. 6) has been consistently observed on both n- and p-type samples and may be attributed to filling of trapping centers in the oxide [28].

2) Accumulation: The frequency dispersion observed in accumulation is caused by oxide layers of relatively low resistivity adjacent to the interface. This reduces the effective oxide thickness and increases the observed capacitance with decreasing measurement frequency (Maxwell–Wagner effect [29]). It also causes an additional component in the G–V measurements which can be described as a series resistance (R_s) loss [27]. The Maxwell–Wagner effect can be approximated by an equivalent circuit comprising multiple RC circuits connected in series. The equivalent circuit parameters have been inferred from C–V and G–V measurements in accumulation. For the C–V and G–V results shown in Figs. 6 and 7, respectively, the nonuniformity extends over a depth of $\cong$ 10 nm from the interface and may be related to the depth profile of the Gd concentration (see Section III). The incorporation of Gd gives also rise to trapping effects and



(a)



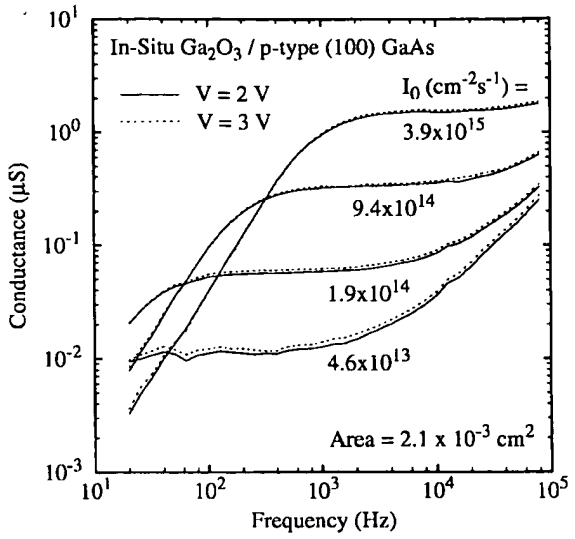
(b)

Fig. 7. Typical G–V characteristics of *in situ* fabricated Ga_2O_3–GaAs (a) n-type and (b) p-type samples. The oxide thickness t_{ox} is 46.2 and 59.4 nm, respectively. The substrate deposition temperature $T_s \cong 600$ °C, the light intensity during the measurement $I_0 = 9.4 \times 10^{14}$ cm^{-2} s^{-1}.

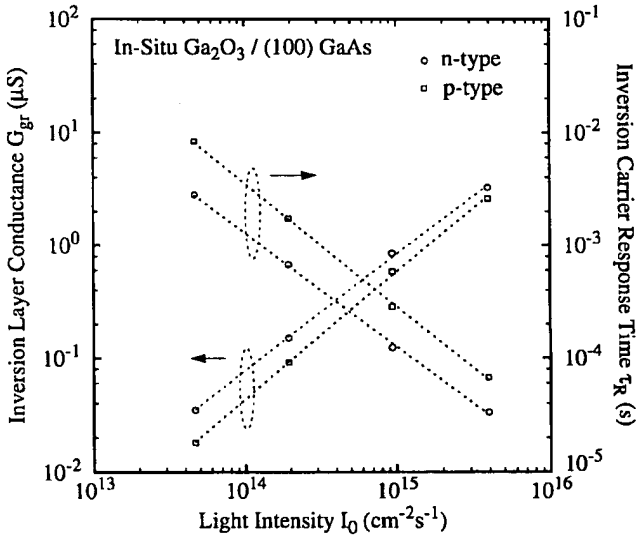
charge injection into the oxide which cause long term drift of the capacitance and of device parameters in accumulation [28].

Another interesting feature disclosed in Fig. 6(a) is the quasi-static capacitance being typically smaller in accumulation than in inversion. This is attributed to the low effective density of states in the GaAs conduction band compared to that of the valence band. This characteristic feature has been experimentally observed for the first time and confirmed by calculations based on our selfconsistent device model for semiconductor heterostructures.

3) Depletion: We have inferred D_{it} using results of C–V and G–V measurements in depletion. Fig. 9 shows typical results obtained for D_{it} as a function of bandgap energy. We will first discuss D_{it} obtained from C–V measurements using the quasi-static/high-frequency technique [27]. D_{it} indicated



(a)



(b)

Fig. 8. (a) Measured conductance G as a function of frequency with I_0 as a parameter for the *in situ* fabricated Ga_2O_3/p-type GaAs structure of Fig. 7(b) in strong inversion. (b) G_{gr} and τ_R as a function of I_0 for the *in situ* fabricated Ga_2O_3–GaAs structures of Fig. 7 in strong inversion.

by open circles and triangles has been derived from p- and n-type samples, respectively. The inferred midgap interface state density D_{it} is in the low 10^{10} cm^{-2} eV^{-1} range. Note that the quasi-static/high-frequency technique requires conclusive evidence that interface traps do not respond to the high-frequency signal. This has been clearly demonstrated in Fig. 6 which shows virtually identical measurement results in depletion above measurement frequencies of 1 kHz.

Further, we have thoroughly studied the effect of low-intensity light illumination and its implications for the derivation of D_{it}. The application of low-intensity light illumination during the measurement causes the electron quasi-Fermi level E_{Fn} to depart from the hole quasi-Fermi level E_{Fp} in the semiconductor and modifies the quasi-static and high-frequency C–V curves. This is demonstrated in Fig. 10

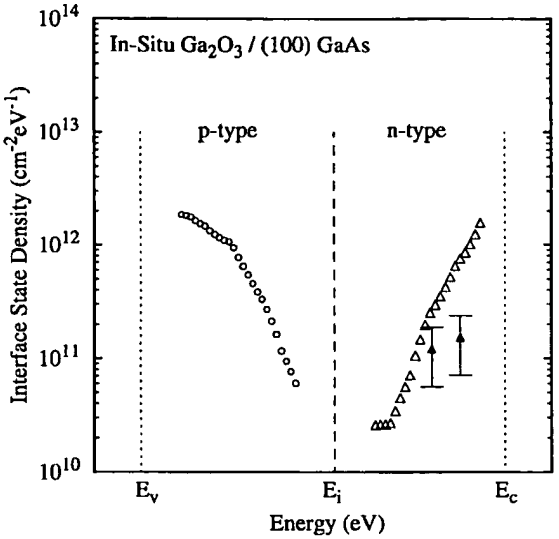


Fig. 9. Typical D_{it} as a function of bandgap energy for *in situ* fabricated Ga_2O_3–GaAs interfaces. The open circles and triangles have been obtained from the quasi-static and 1 MHz C–V measurements shown in Fig. 6 (corrected for the Maxwell–Wagner effect [29]), the filled triangles have been inferred from G–V measurements of another *in situ* fabricated Ga_2O_3/n-type GaAs structure.

for a Ga_2O_3/n-type GaAs structure. Two consequences of illumination on the derivation of D_{it} have been revealed. Since $E_{Fn} \neq E_{Fp}$, 1) weak inversion already occurs for $E_{Fn} > E_i$ (n-type, see Fig. 10) or $E_{Fp} < E_i$ (p-type), and 2) the occupancy of all interface states located at E_t between E_{Fn} and E_{Fp} is changed when $(E_{Fn} + E_{Fp})/2$ crosses the midgap level E_i. Whereas the first implication only restricts the validity range of the quasi-static/high-frequency technique to $E > E_i + 0.17$ eV (n-type) and $E < E_i - 0.17$ eV (p-type) in our experiments, the second effect can lead to an artificially high result for D_{it}. With respect to the latter finding, the inferred midgap D_{it} should be considered as an upper limit. More details on the effects of low-intensity light illumination on C–V characteristics will be reported in [25].

For G–V analysis, our measurement results need to be corrected for R_s [27]. Fig. 11 shows the R_s corrected high-frequency G–V curves for a Ga_2O_3/n-type GaAs structure. Note that the corrected curves shown in Fig. 11 were not obtained from the G–V results shown in Fig. 7 since interface trap loss is entirely masked by oxide loss (R_s) for the latter G–V curves. Using the corrected G–V curves, D_{it} is obtained using

$$D_{it} \cong \frac{G_p}{Aq^2 f_D \omega \{(C_{ox} - C_p)/C_{ox}\}^2} \tag{4}$$

where A, f_D, G_p, C_p, and q are the sample area, a universal function ($f_D \cong 0.12 - 0.4$), the measured conductance and capacitance at the conductance peak [27], and the electronic charge. Using (4), $D_{it} = (1.2 \pm 0.7) \times 10^{11}$ and $(1.5 \pm 0.8) \times 10^{11}$ cm^{-2} eV^{-1} have been obtained in the vicinity of the conduction band edge for $E = E_c - 0.29$ eV and $E = E_c - 0.17$ eV, respectively (filled triangles in Fig. 9). The relatively large error range for D_{it} stems from the

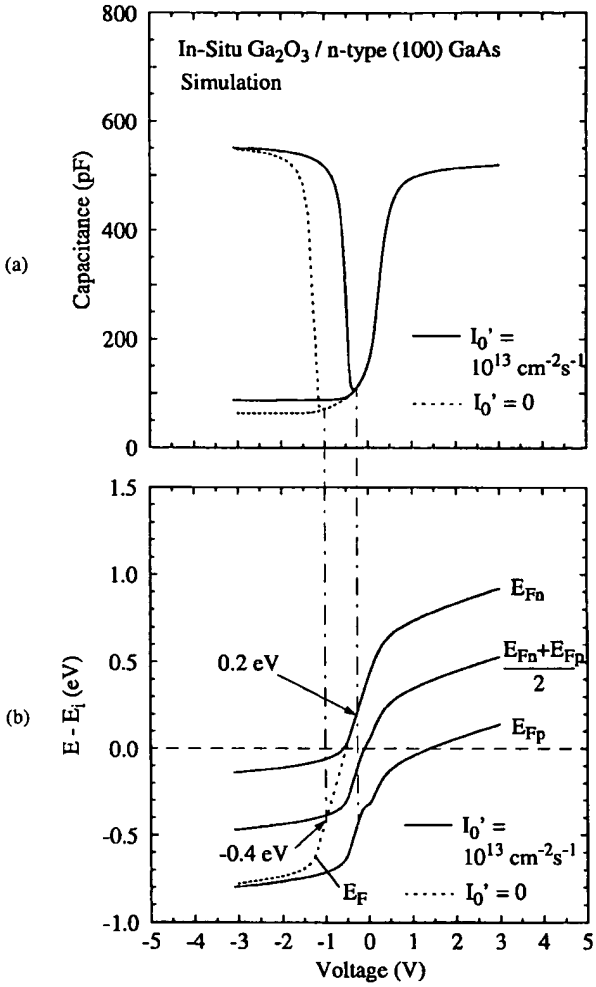


Fig. 10. Calculated (a) quasi-static and high-frequency C–V and (b) Fermi level with E as a parameter as a function of voltage for no light ($I_0' = 0$) and low-intensity light entering the semiconductor ($I_0' = 10^{13}$ cm^{-2} s^{-1}).

assumption $0.12 \leq f_D \leq 0.4$ [27]. To accurately determine f_D would require a conductance measurement as a function of frequency which was not performed. Note that the divergence of D_{it} results obtained from G–V and C–V measurements rapidly increases when E_F moves toward E_c. For $E_c - 0.17$ eV, D_{it} is about an order of magnitude higher when determined from C–V curves as compared to G–V results. This is indicative of a slow trapping process in the oxide which is partially reflected by the quasi-static/high-frequency C–V method but is completely invisible in high-frequency G–V measurements. The time constants of charge trapping in the oxide are > 1 s [28] and depend only indirectly on the position of E_F at the semiconductor surface via the carrier concentrations in the semiconductor bands [30].

The interface state density D_{it} is directly related to the interface recombination velocity S (1). Therefore, we performed complementary studies of the internal quantum efficiency η (derived from I_{PL}) from low injection ($\rho < N$) to very high injection ($\rho > N$) over a wide range of incident light power densities $P_0(1 \leq P_0 \leq 10^4$ W/cm^2). Here, ρ is the injected carrier density. This technique is based on the

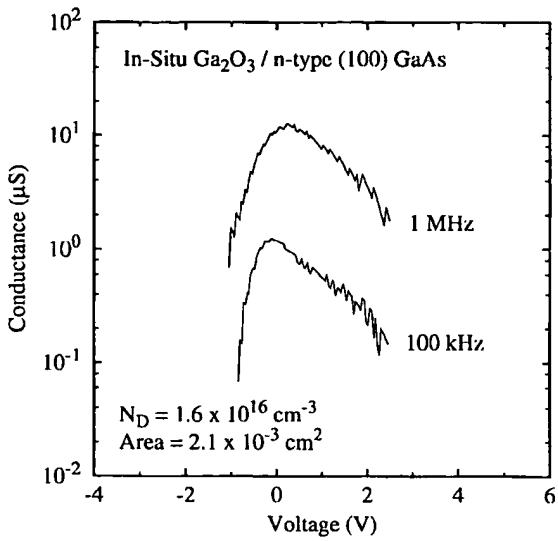


Fig. 11. R_s corrected high-frequency G–V curves for an *in situ* fabricated Ga_2O_3/n-type GaAs structure ($T_s \cong 360$°C).

relative weight of nonradiative (R_{SRH}) and radiative (R_{rad}) recombination as a function of P_0 resulting in a unique curve shape of η versus P_0 for a specific S (see, e.g., [31], [32]). This is demonstrated in Fig. 12(a) which shows the measured (symbols) and simulated (lines) efficiency η versus P_0' of *in situ* and *ex situ* (to be discussed later) fabricated Ga_2O_3/n-type GaAs structures and, for comparison purposes, η versus P_0' of a reference $Al_{0.45}Ga_{0.55}As$–GaAs interface (n-type). Here, $P_0' = TP_0$ where T is the optical transmissivity of the samples and $\lambda_0 = 514.5$ nm is the excitation wavelength. The simulation results have been obtained from calculated PL depth profiles using our self-consistent, numerical interface analysis device model [25], [32]. Note that the analysis has been performed from low to very high injection levels since the calculated carrier densities ρ are 6.5×10^{14} and 7.8×10^{17} cm^{-3} at the semiconductor surface ($S = 5000$ cm/s) for the lowest and highest excitation densities P_0 of 1 and 10^4 W/cm^2, respectively. Since the PL intensity is not measured in absolute units, the measured curves are rigidly shifted to the calculated ones [31]. The best fit of the simulations to the measurement data has been attained for $S = 4000$–5000 and 1000 cm/s for Ga_2O_3– and $Al_{0.45}Ga_{0.55}As$–GaAs structures, respectively. The above obtained S at *in situ* fabricated Ga_2O_3–GaAs interfaces corresponds to a capture-cross section σ of $\cong 10^{-15}$ cm^2. Further, Fig. 12(b) shows η versus P_0' of *in situ* fabricated Ga_2O_3/p-type GaAs structures. Here, the inferred recombination velocity S is $\cong 10^4$ cm/s. In contrast to the results on n-type samples, η does not saturate for very high injection levels and exhibits a weaker dependence on P_0'. The observed differences in the η–P_0' characteristics for n- and p-type samples are discussed in [25], [32].

B. Ex Situ Deposited Ga_2O_3–GaAs Interfaces

The *in situ* process requires complex equipment and moreover, it is not applicable to electronic passivation of GaAs surfaces exposed to processing environments during device

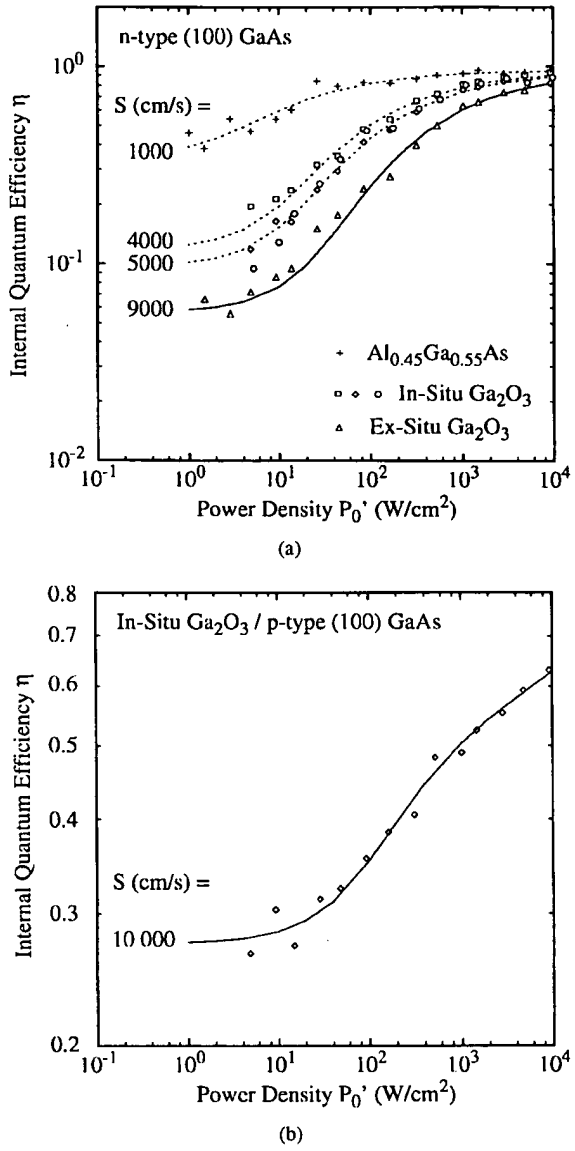


Fig. 12. (a) Measured (symbols) and calculated (lines) internal quantum efficiency η of *ex situ* and *in situ* fabricated Ga_2O_3/n-type GaAs samples and for a conventional $Al_{0.45}Ga_{0.55}As$–GaAs structure as a function of P_0'. For *in situ* fabricated interfaces, squares, diamonds, and circles represent results measured for T_s = 360, 550, and 620 °C, respectively. (b) Measured (symbols) and calculated (line) η of *in situ* fabricated Ga_2O_3/p-type GaAs samples (T_s = 560 °C).

fabrication. Our *ex situ* technique, however, provides excellent passivation for GaAs wafers or surfaces exposed to room air and/or processing environments during fabrication of devices. The first *ex situ* fabricated Ga_2O_3/n-type GaAs interfaces are inferior (when compared to *in situ* Ga_2O_3–GaAs interfaces) but still of a high quality with S = 9000 cm/s [see Fig. 12(a), triangles, $T_s \cong 480$ °C]. Using (1), a corresponding D_{it} in the upper 10^{10} cm^{-2} eV^{-1} range is derived.

Note that the requirement of extremely low GaAs surface exposure as outlined in Section I demands GaAs surface preparation in ultrahigh vacuum prior to oxide deposition for the *ex situ* approach as well. All other attempts to clean the surface outside the UHV chamber prior to Ga_2O_3 deposition

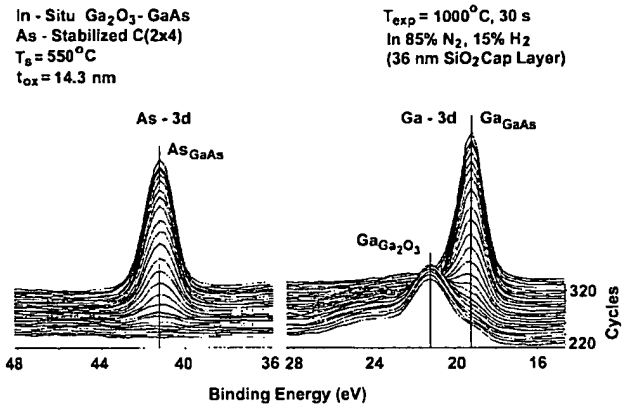


Fig. 13. Interfacial depth profiles of Ga and As 3d core levels of *in situ* fabricated Ga_2O_3–GaAs structures after RTA in forming gas (15% H_2, 85% N_2) at 1000 °C for 30 s.

did not produce any improvements of electrical interface properties compared to a bare sample [25]. Clearly, UHV surface preparation is an indispensable ingredient for low D_{it} insulator–GaAs interfaces.

V. Interface Stability

Stability of interfaces is of paramount importance for electronic and optoelectronic device and circuit fabrication and operation as well. Interface degradation is observed when thermal or optical energy levels exceed the bond strength of interfacial atomic bonds. Since thermodynamically and photochemically induced interface degradation rely on similar mechanisms, the demonstration of photochemical stability confirms the evidence provided by thermodynamic stability. Therefore, we have investigated both thermodynamic and photochemical interface stability.

We have performed first studies on the thermodynamic stability of *in situ* fabricated Ga_2O_3–GaAs interfaces for temperature stress of up to 1000 °C. Structural and electronic interface properties after temperature stress have been investigated and compared to as deposited interfaces. Further, the photochemical interface stability of as deposited and temperature stressed interfaces has been examined using high-intensity laser excitation.

A. Thermodynamic Stability

Fig. 13 shows typical interfacial depth profiles of Ga and As 3d core levels of *in situ* fabricated Ga_2O_3–GaAs structures after rapid thermal annealing (RTA) in forming gas (15% H_2, 85% N_2) at 1000 °C for 30 s. The Ga and As 3d binding energies of $Ga_{Ga_2O_3}$, Ga_{GaAs}, and As_{GaAs} are 21.2, 19.2, and 41.2 eV, respectively, and remain unchanged after temperature stress [see Fig. 5(a)]. Like for As deposited interfaces, chemical reaction products, in particular As_2O_3 (44.6 eV) and As_2O_5 (45.7 eV) are not detectable at temperature stressed Ga_2O_3–GaAs interfaces. The excellent thermodynamic stability is consistent with predictions based on thermochemical phase diagrams published by Schwartz in 1983 [9], and has important implications for the stability of electronic interface

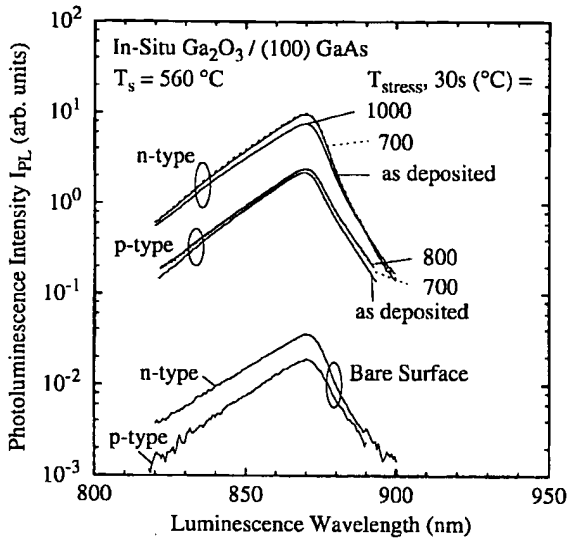


Fig. 14. Typical PL spectra of *in situ* fabricated n- and p-type as deposited (T_s = 560 °C) and temperature stressed Ga_2O_3–GaAs structures as well as of corresponding bare samples.

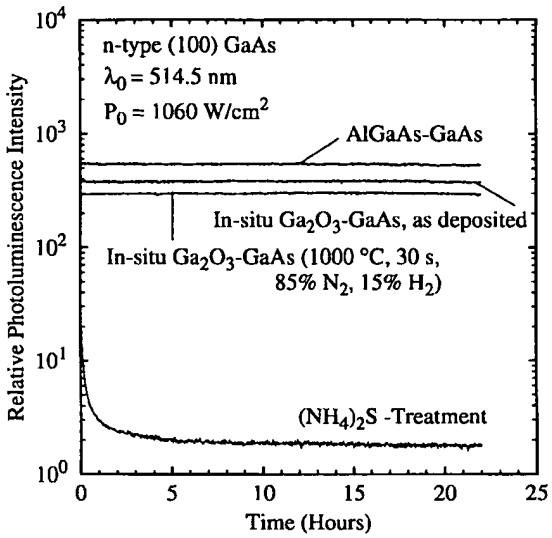


Fig. 15. Measured PL as a function of time normalized to the PL of a corresponding bare surface (at zero time) for *in situ* fabricated Ga_2O_3–GaAs interfaces, $Al_{0.45}Ga_{0.55}As$–GaAs structures, and Si_3N_4–GaAs samples using $(NH_4)_2S$ treatment and ECR plasma deposition. All samples comprise identical GaAs epitaxial layers and substrates.

properties to be discussed later. Note that a 36-nm thick SiO_2 cap layer has been deposited prior to rapid thermal annealing in order to avoid interface degradation caused by penetrating gas species. This relatively thick SiO_2 layer introduces additional surface roughness in the course of sputtering and in turn, decreases the height and increases the spatial extension (not shown) of the acquired $Ga_{Ga_2O_3}$ spectra.

Electronic interface properties of temperature stressed, *in situ* fabricated Ga_2O_3–GaAs interfaces have been investigated by standard steady-state PL measurements. Fig. 14 shows typical PL spectra of n- and p-type as-deposited and temperature stressed Ga_2O_3–GaAs structures as well as of the corresponding bare samples. The incident light power density P_0 and the excitation wavelength λ_0 are 1060 W/cm^2 and 514.5 nm, respectively. As indicated in Fig. 14, the PL spectra after RTA in forming gas for 30 s at 700 or 800 °C are virtually identical to those obtained from corresponding as-deposited samples. These results imply preservation of excellent electronic interface properties. I_{PL} decreases by only 21% after temperature stress of 1000 °C for 30 s giving a slightly increased recombination velocity $S \cong 8500$ cm/s. Note that identical results have been obtained after temperature stress in inert gases such as N_2.

B. Photochemical Stability

Fig. 15 shows the relative peak photoluminescence intensity of *in situ* fabricated n-type Ga_2O_3–GaAs samples and of an n-type $Al_{0.45}Ga_{0.55}As$–GaAs reference structure as a function of time t measured for a high-incident light power density $P_0 = 1060$ W/cm^2. Here, the unit *relative photoluminescence* is defined as the PL intensity of the structures under test normalized to the PL of a corresponding bare surface at zero time determined at $P_0 = 1060$ W/cm^2. Furthermore, the as-measured PL signals have been corrected for alterations of optical transmissivity T. The slope of the measured PL versus time characteristics is +0.028, +0.041, and −0.079%/h for as-deposited and temperature stressed Ga_2O_3–GaAs interfaces, and for the $Al_{0.45}Ga_{0.55}As$–GaAs reference structure, respectively. Thus, *in situ* fabricated Ga_2O_3–GaAs interfaces show excellent photochemical stability with no degradation of PL intensity to be observed after 22 h of high-intensity laser excitation. These results imply preservation of excellent interface properties in agreement with the conclusions obtained from the above described temperature stress experiments.

For comparison purposes, an optimized $(NH_4)_2S$ treatment of a GaAs surface combined with electron cyclotron resonance (ECR) plasma deposition of Si_3N_4 and subsequent annealing has been performed on n-type bare reference samples. Fig. 15 also shows the best result obtained using the latter technique. In sharp contrast to *in situ* fabricated Ga_2O_3–GaAs interfaces, the relative PL intensity of $(NH_4)_2S$ treated samples decays rapidly from 20 to 2.7 during the first hour of high-intensity light exposure. Note that the relatively low PL of the $(NH_4)_2S$ treated sample measured at zero time is indicative of $S \cong 10^5$ cm/s for an As-deposited structure.

VI. Summary

The extension of MBE toward deposition of gallium oxide molecules has provided required ingredients for the implementation of thermodynamically stable, low D_{it} oxide–GaAs interfaces for low-power, GaAs-based applications. The following results have been obtained.

1) Excellent electronic interface properties including D_{it} in the low 10^{10} cm^{-2} eV^{-1} range and $S = 4000$–5000 cm/s for *in situ* fabricated Ga_2O_3–GaAs interfaces, and D_{it} in the upper 10^{10} cm^{-2} eV^{-1} range and $S = 9000$ cm/s for *ex situ* fabricated Ga_2O_3–GaAs interfaces.
2) Strong inversion in both n- and p-type GaAs.

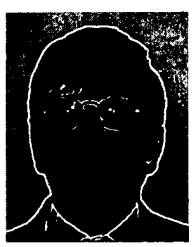
3) Thermodynamic interface stability up to at least 800 °C and photochemical interface stability.
4) Charge trapping in the oxide has been revealed as the dominant trapping mechanism. Alternative Ga_2O_3 deposition techniques need to be explored to further reduce the total density of trapping centers in the structure and to eliminate the Maxwell–Wagner effect observed in accumulation.

ACKNOWLEDGMENT

M. Hong and J. P. Mannaerts gratefully acknowledge A. Y. Cho for his support and technical discussions.

REFERENCES

[1] A. Chandrashekaran and R. Broderson, "Low-power CMOS digital design," *IEEE J. Solid-State Circuits,* vol. 27, pp. 473–484, April 1992.
[2] G. Schrom, C. Pichler, T. Simlinger, and S. Selberherr, "On the lower bounds of CMOS supply voltage," *Solid-State Electron.,* vol. 39, pp. 425–430, 1996.
[3] W. M. Huang, K. Papworth, M. Racanelli, J. P. John, J. Foerstner, H. C. Shin, H. Park, B. Y. Hwang, T. Wetteroth, S. Hong, H. Shin, S. Wilson, and S. Cheng, "TFSOI CMOS technology for sub 1 V microcontroller circuits," in *IEDM Tech. Dig.,* 1995, pp. 59–62.
[4] P. K. Vasudev, "CMOS device and interconnect technology enhancements for low-power/low-voltage applications," *Solid-State Electron.,* vol. 39, pp. 481–488, 1996.
[5] D. E. Fulkerson, S. Baier, J. Nohava, and R. Hochhalter, "Complementary heterostructure FET technology for low-power, high-speed digital applications," *Solid-State Electron.,* vol. 39, pp. 461–469, 1996.
[6] B. Bernhardt, M. LaMacchia, J. Abrokwah, J. Hallmark, R. Lucero, B. Mathes, B. Crawforth, D. Foster, K. Clauss, S. Emmert, T. Lien, E. Lopez, V. Mazzotta, and W. Ooms, "Complementary GaAs (CGaAs^{TM}): A high-performance BiCMOS alternative," in *IEEE GaAs Symp. Tech. Dig.,* 1995, pp. 18–21.
[7] M. Passlack, M. Uhle, and H. Elschner, "Analysis of propagation delays in high-speed VLSI circuits using a distributed line model," *IEEE Trans. Computer-Aided Design,* vol. 9, pp. 821–826, Aug. 1990.
[8] W. E. Spicer, I. Lindau, P. Skeath, C. Y. Su, and P. Chye, "Unified defect model and beyond," *J. Vac. Sci. Technol.,* vol. 17, pp. 1019–1027, 1980.
[9] G. P. Schwartz, "Analysis of native oxide films and oxide-substrate reactions on III–V semiconductors using thermochemical phase diagrams," *Thin Solid Films,* vol. 103, pp. 3–16, 1983.
[10] O. Kubaschewski and C. B. Alcock, *Metallurgical Thermochemistry.* Oxford U.K.: Pergamon, 1979.
[11] J. M. Woodall and J. L. Freeouf, "GaAs metallization: Some problems and trends," *J. Vac. Sci. Technol.,* vol. 19, pp. 794–798, 1981.
[12] M. Passlack and M. Hong, "Low interface state density oxide–GaAs structures fabricated by *in situ* molecular beam epitaxy," in *Proc. MRS Spring Mtg.,* Materials Research Society, San Francisco, CA, 1996, vol. 421 (Compound Semiconductor Electronics and Photonics).
[13] M. Hong, "New frontiers of molecular beam epitaxy with *in situ* processing," *J. Cryst. Growth,* vol. 150, pp. 277–284, 1995.
[14] R. Ludeke and A. Koma, "Surface studies on clean and oxygen exposed GaAs and Ge surfaces by low-energy electron loss spectroscopy," *CRC Crit. Rev. Solid-State Sci.,* vol. 5, p. 259, 1975.
[15] M. Hong, M. Passlack, J. P. Mannaerts, T. D. Harris, M. L. Schnoes, R. L. Opila, and H. W. Krauttner, "A Ga_2O_3 passivation technique compatible with GaAs device processing," *Solid-State Electron.,* accepted for publication.
[16] W. Piekarczyk and A. Pajaczkowska, "Dissociation process and crystal growth of gadolinium gallium garnet," *J. Cryst. Growth,* vol. 46, pp. 483–486, 1979.
[17] M. Passlack, E. F. Schubert, W. S. Hobson, M. Hong, N. Moriya, S. N. G. Chu, K. Konstadinidis, J. P. Mannaerts, M. L. Schnoes, and G. J. Zydzik, "Ga_2O_3 films for electronic and optoelectronic applications," *J. Appl. Phys.,* vol. 77, pp. 686–693, 1995.
[18] *CRC Handbook of Chemistry and Physics,* 76th ed. Boca Raton, FL: CRC, 1995, pp. 4–58.
[19] M. Passlack, M. Hong, E. F. Schubert, J. R. Kwo, J. P. Mannaerts, S. N. G. Chu, N. Moriya, and F. A. Thiel, "*In situ* fabricated Ga_2O_3–GaAs structures with low interface recombination velocity," *Appl. Phys. Lett.,* vol. 66, pp. 625–627, 1995.
[20] S. Tanuma, C. J. Powell, and D. R. Pen, "Calculations of electron inelastic mean free paths," *Surf. Interface Anal.,* vol. 17, pp. 927–939, 1991.
[21] Y. Mizokawa, H. Iwasaki, R. Nishitani, and S. Nakamura, "Quantitative chemical depth profiles of anodic oxide on GaAs obtained by X-ray photoelectron spectroscopy," *J. Electrochem. Soc.: Solid-State Sci. Technol.,* vol. 126, pp. 1370–1374, 1979.
[22] M. Passlack, M. Hong, R. L. Opila, J. P. Mannaerts, and J. R. Kwo, "GaAs surface passivation using *in situ* oxide deposition," *Appl. Surf. Sci.,* vols. 104/105, pp. 441–447, 1996.
[23] R. K. Ahrenkiel and M. S. Lundstrom, *Minority Carriers in III–V Semiconductors: Physics and Applications.* Boston MA: Academic, 1993, pp. 48, 54, 58, 119–121, and 129–134.
[24] M. S. Lundstrom and R. J. Schuelke, "Numerical analysis of heterostructure semiconductor devices," *IEEE Trans. Electron Devices,* vol. ED-30, pp. 1151–1159, Sept. 1983.
[25] M. Passlack, M. Hong, J. P. Mannaerts, E. F. Schubert, G. J. Zydzik, W. S. Hobson, and T. D. Harris, "Advancing metal-oxide-semiconductor theory: Steady-state nonequilibrium conditions," submitted for publication.
[26] M. Hong, M. Passlack, J. P. Mannaerts, J. R. Kwo, S. G. N. Chu, N. Moriya, S. Y. Hou, and V. J. Fratello, "Low interface state density oxide–GaAs structures fabricated by *in situ* molecular beam epitaxy," *J. Vac. Sci. Technol. B,* vol. 14, pp. 2297–2300, 1996.
[27] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology.* New York: Wiley, 1982, pp. 104–156, 176–222, 222–226, and 331–333.
[28] M. Passlack, M. Hong, and J. P. Mannaerts, "Quasi-static and high-frequency capacitance voltage characterization of Ga_2O_3–GaAs structures fabricated by *in situ* molecular beam epitaxy," *Appl. Phys. Lett.,* vol. 68, pp. 1099–1101, 1996.
[29] A. R. von Hippell, *Dielectrics and Waves.* New York: Wiley, 1954, p. 412.
[30] F. P. Heiman and G. Warfield, "The effects of oxide traps on the MOS capacitance," *IEEE Trans. Electron Devices,* vol. ED-12, pp. 167–178, Apr. 1965.
[31] O. Brandt, K. Kanamoto, M. Gotoda, T. Isu, and N. Tsukada, "Comparative analysis of the optical quality of single $In_{0.1}Ga_{0.9}As$–$Al_{0.33}Ga_{0.67}As$ quantum wells grown by molecular beam epitaxy on (100) and (311) GaAs substrates," *Appl. Phys. Lett.,* vol. 67, pp. 1885–1887, 1995.
[32] M. Passlack, M. Hong, J. P. Mannaerts, J. R. Kwo, and L. W. Tu, "Recombination velocity at oxide-GaAs interfaces fabricated by *in situ* molecular beam epitaxy," *Appl. Phys. Lett.,* vol. 68, pp. 3605–3607, 1996.



M. Passlack (M'93) received the Dipl.-Ing. degree in 1984, the Dr.-Ing. degree in 1988, and the Dr.-Ing. habil. degree in 1990, all in electrical engineering from Technische Universität Dresden, Germany.

From 1984 to 1988, he worked on modeling, design, simulation, and characterization of GaAs devices and integrated circuits. He was an Assistant Professor and the Principal Investigator of a research project on multiple-state quantum functional devices and integrated circuits from 1989 to 1991 at Technische Universität Dresden. In 1992, he was with the Daimler–Benz Research Center, Ulm, Germany, where he worked on thermal modeling of GaAs power HBT's. From 1993 to 1995, he was engaged in research activities on insulator-GaAs interfaces and 980-nm high-power pump lasers at AT&T Bell Laboratories, Murray Hill, NJ. In 1995, he joined the Motorola Phoenix Corporate Research Laboratories, Tempe, AZ, where he is currently working on insulator-GaAs interfaces and GaAs heterostructure devices.

M. Hong (M'83) received the B.S. degree in physics from National Taiwan University, Taipei, in 1973. After a two-year military service in Taiwan's navy, he attended the University of California, Berkeley, where he received the M.S. and Ph.D. degrees in materials science and engineering in 1978 and 1980, respectively.

From 1980 to 1981, he was a Staff Scientist II at Lawrence Berkeley Laboratory, where he was in charge of a superconducting material program for applications in high-energy physics accelerator and fusion reactor magnets. In 1981, he joined the Materials Research Laboratory, Bell Laboratories, Murray Hill, NJ, where he was engaged in research activities of A15 superconductors, magnetic rare earth superlattices, magnetic thin films for magneto-optical recording, and high-temperature superconductivity. In 1988, he joined the Semiconductor Research Laboratory, Bell Laboratories, where he has developed an *in situ* process combining MBE of III–V compound semiconductors, metals, and oxides with electron cyclotron resonance (ECR) plasma etching.

J. P. Mannaerts, photograph and biography not available at the time of publication.

R. L. Opila (M'83) received the B.S. degree in chemistry from the University of Illinois, Champaign-Urbana, in 1975, and the Ph.D. degree in physical chemistry from the University of Chicago, Chicago, IL, in 1982.

He joined AT&T Bell Laboratories, Murray Hill, NJ, in 1982 as a Member of Technical Staff in the Materials Science Division. In 1993, he was promoted to Distinguished Member of Technical Staff. Currently, he is a Technical Manager at Bell Laboratories, Lucent Technologies, (formerly AT&T Bell Laboratories), and manages the Surface Preparation and Interface Reliability Group.

S. N. G. Chu received the B.S. degree in physics from National Taiwan University, Taipei, and the M.S. and Ph.D. degrees in materials science from the University of Rochester, Rochester, NY.

He joined AT&T Bell Laboratories, Murray Hill, NJ, in 1980 and has been associated with fiber-optic communications technology working on various compound semiconductor materials, device structures, and reliability. Currently, he is a Distinguished Member of the Technical Staff in the Quantum Phenomena and Device Research Department, Bell Laboratories, Lucent Technologies, Murray Hill, NJ, working on materials for high-speed electronic devices for wireless applications. He has published over 230 papers in major journals, and holds three patents in these areas.

Dr. Chu is a Fellow of The Electrochemical Society and has been active in the Electrochemical Society affairs. He is also a member of the American Physical Society, ASM International, the Mineral, Metal, and Materials Society, and the Materials Research Society.

N. Moriya received the M.S. and Ph.D. degrees in physics from the Technion–Israel Institute of Technology, Haifa, in 1988 and 1991, respectively.

From 1992 to 1995, he was with AT&T Bell Laboratories, Murray Hill, NJ, where he investigated diffusion and bandgap effects in strained semiconductor layers. Currently, he is with Netmor Ltd.—Applied Modeling Research, Tel Aviv, Israel, where he is involved with research and development in the area of virtual reality. His research and interest areas include detection methods and numerical simulation for complex systems.

F. Ren (SM'93), photograph and biography not available at the time of publication.

J. R. Kwo received the B. S. degree in physics from National Taiwan University, Taipei, in 1975, and the M.S. and Ph.D degrees in applied physics from Stanford University, Stanford, CA, in 1977 and 1981, respectively.

In 1981, she joined AT&T Bell Laboratories, Murray Hill, NJ, as a Member of Technical Staff in the basic research area. Since joining Bell Laboratories, her work has been primarily on thin-film synthesis of a variety of novel electronic materials. She was a pioneer in developing metal molecular beam epitaxy (MBE) methods for epitaxial growth of metallic superlattices during 1982–1986. Her work on synthetic rare earth magnetic superlattices demonstrated the modulation effect in magnetic properties through artificial layering for the first time. A variety of new, coherent magnetic order was discovered in the artificial magnetic heterostructures. From 1987 to 1992, she worked on high-temperature superconducting (HTSC) oxide films by both MBE and sputtering methods for studying superconducting and transport properties as well as for HTSC devices. In recent years, her interest has shifted toward investigating new transparent oxide films for electrophoto applications, and high dielectric constant films for charge.